IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please AMEND paragraphs [0013], [0048], and [0060] in accordance with the following:

[0013] Address data and data that are input from a predetermined element 160 of a system 150, such as an interface or a central processing unit ~~(CPU, not shown)~~ (CPU) via a system bus ~~(not shown)~~ 170 are sequentially latched by the address latch 101 and the data latch 103, respectively. The latched address data are divided into a column address and a row address, and then the column address and the row address are encoded separately. Thereafter, the encoded column address and the encoded row address are sequentially stored in an address queue, i.e., the memory address queue 102. An upper module 180, a lower module 190, and a system element 160 are coupled to system bus 170.

[0048] The address latch 401 latches address data input into the memory controller 400 from an upper module ~~(not shown)~~ 480 of a system 450. A system element 460, the upper module 480, and a lower module 490 are coupled to system bus 470. Examples of a system element 460 include an interface or a central processing unit.

[0060] The read data queue 604 sequentially stores the read data output from the memory module 610 via a data line 607 connecting the memory controller 600 and the memory module 610 and transmits the stored data to the upper module ~~(not shown)~~ 680 of the system 650 via the data latch 602. A system element 660, the upper module 680, and a lower module 690 are coupled to system bus 670. Examples of a system element 660 include an interface or a central processing unit.